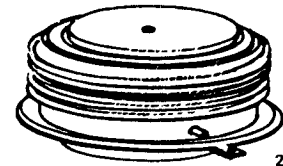


276

INVERTER SCR's 700 TO 1500 AMPERES



276.1

GE TYPE	C648	C612	C613	C712
CONSTRUCTION	AMPLIFYING GATE	AMPLIFYING GATE	AMPLIFYING GATE	AMPLIFYING GATE
ELECTRICAL SPECIFICATIONS				
VOLTAGE RANGE	500-1200	1500-1800	1800-2000	1500-2000
FORWARD CONDUCTION				
$I_{T(RMS)}$	Max. forward conduction sinusoidal @ $T_C = 65^\circ C$, 50% duty (A)			
@ 60 Hz	1150	700	800	1500
@ 600 Hz	1150	700	800	1500
@ 1200 Hz	1150	—	800	1500
@ 2500 Hz	1100	—	760	1500
@ 5000 Hz	1100	—	675	1100
I_{TSM}	Max. peak one cycle, non-repetitive surge current (A)			
	10,000	6500	6500	20,000
$I^2 t$	Max. $I^2 t$ for fusing for 5 to 8.3 msec ($A^2 \text{ sec}$)			
	415,000	150,000	80,000	1,660,000
$R_{\theta JC}$	Max. thermal impedance ($^\circ C/W$)			
	.04	.04	.04	.023
$t_d + t_r$	Typical turn-on time (μsec)			
	2.5	2.0	—	—
t_q	Turn-off time @ rated voltage and T_J $V_R = 50V \text{ min.}$ (μsec) @ 20V/ μsec			
	—	—	—	—
	@ 200V/ μsec reapplied			
	—	—	40	50
	@ 400V/ μsec reapplied			
	40	60	40	—
di/dt	Critical rate-of-rise of on-state current ($A/\mu\text{sec}$)			
	800	500	500	800
T_J	Junction operating temperature range ($^\circ C$)			
	-40 to 125 $^\circ C$	-40 to 125 $^\circ C$	-40 to 125 $^\circ C$	-40 to 125 $^\circ C$
BLOCKING				
dv/dt	Min. critical rate-of-rise of off-state voltage exponential to rated V_{DRM} @ Max. T_J ($V/\mu\text{sec}$)			
	400	200	400	500
FIRING				
I_{GT}	Max. required gate current to trigger (mA) @ -40 $^\circ C$			
	350	200 Typ	200	200
	@ 125 $^\circ C$			
	100	125 Typ	30	30
V_{GT}	Max. required voltage to trigger (V) @ -40 $^\circ C$			
	5	5	5	5
	@ 125 $^\circ C$			
	3	3	3	3
VOLTAGE TYPES				
Repetitive Peak Forward and Reverse Voltages				
100	—	—	—	—
200	—	—	—	—
300	—	—	—	—
400	—	—	—	—
500	C648E	—	—	—
600	C648M	—	—	—
700	C648S	—	—	—
800	C648N	—	—	—
900	C648T	—	—	—
1000	C648P	—	—	—
1100	C648PA	—	—	—
1200	C648PB	—	—	—
1300	—	—	—	—
1400	—	—	—	—
1500	—	C612PE	C613PE	C712PE
1600	—	C612PM	C613PM	C712PM
1700	—	C612PS	C613PS	C712PS
1800	—	C612PN	C613PN	C712PN
1900	—	—	C613PT	C712PT
2000	—	—	C613L	C712L
PACKAGE TYPE	1" PRESS PAK	1" PRESS PAK	1" PRESS PAK	1" PRESS PAK
PACKAGE OUTLINE NO.	276	276	276	276.1

High Speed Silicon Controlled Rectifier

1000 A Avg. Up to 2000 Volts

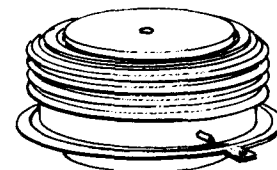
C712



The General Electric device type C712 is a new pressure-mounted, high current SCR designed for power switching at high voltage and high frequencies (up to 5 KHz). The C712 gate structure has an involute, interdigitated pattern to optimize the turn-on area for high di/dt capability and it is processed using a newly developed multi-diffusion technology.

FEATURES:

- Off-State and Reverse Blocking Capabilities to 2000 Volts.
- Very Low Switching Losses at High Frequencies.
- 60 μ sec Maximum Turn-Off Time at Severe Operating Conditions with Feedback diode.
- Involute, Interdigitated Gate for High di/dt Capability.
- Narrow Pulse Capability for PWM Inverter Commutating SCR Socket.
- 1" Creepage-Path, Glazed-Ceramic Package.



IMPORTANT: Mounting instructions on the last page of C702 specification must be followed.

MAXIMUM ALLOWABLE RATINGS

TYPE	V _{DRM} /V _{RRM} ¹ REPETITIVE T _J = -40°C to +125°C	V _{DRM} /V _{RRM} ¹ REPETITIVE T _J = 0°C to +125°C	TRANSIENT PEAK REVERSE VOLTAGE, V _{RSM} ¹ T _J = -40°C to +125°C
C712L	2000 Volts	2100 Volts	2100 Volts
C712PT	1900	2000	2000
C712PN	1800	1900	1900
C712PS	1700	1800	1800
C712PM	1600	1700	1700
C712PE	1500	1600	1600

Consult factory for lower rated voltage devices.

Peak One-Cycle Surge On-State Current, I _{TSM} (8.3 msec)	20,000 Amperes
Maximum Rate-of-Rise of Anode Current Turn-On Interval (Switching From 1200 Volts)	800 A/ μ sec
Repetitive di/dt Rating ²	200 A/ μ sec
I ² t (for fusing) (at 8.3 milliseconds)	1,660,000 Ampere ² Seconds
Peak Gate Power Dissipation, P _{GM}	100 Watts
Average Gate Power Dissipation, P _{G(AV)}	5 Watts
Peak Reverse Gate Voltage, V _{GRM}	20 Volts
Storage and Operating Temperature, T _{STG} and T _J	-40°C to +125°C
Mounting Force Required	5000 Lb. + 1000 - 0 Lb. 22.2 KN + 4.4 - 0 KN

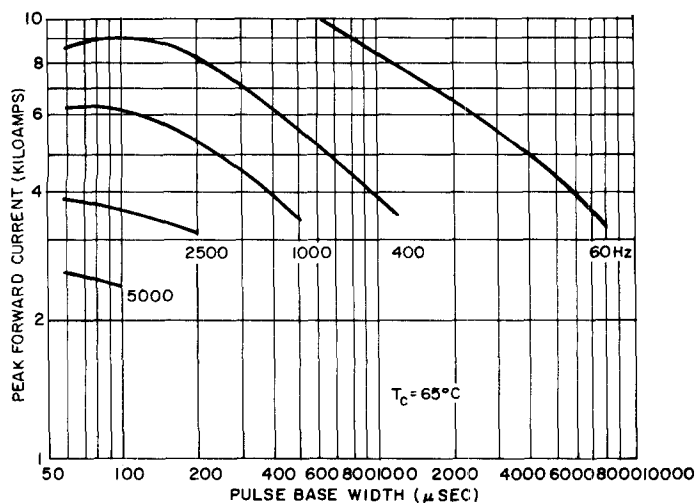
NOTES:

¹ 10 msec voltage sinewave.

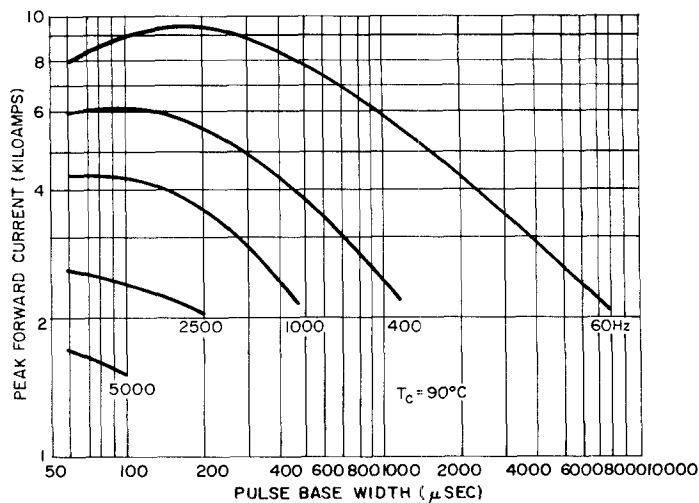
² di/dt rating established in accordance with EIA-NEMA Standard RS-397, Section 5.2.2. This di/dt is in addition to the discharge of a 0.25 μ f, 20 ohm snubber circuit in parallel with the DUT.

CHARACTERISTICS

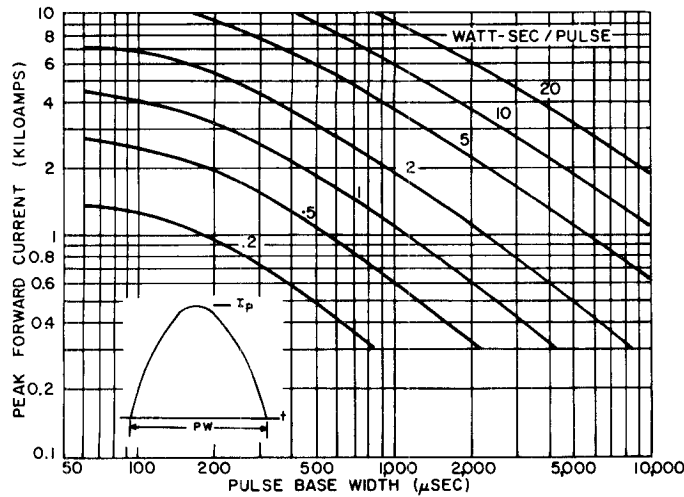
C712	TEST	SYMBOL	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
	Peak Reverse and On-State Blocking Current	I_{DRM} and I_{RRM}	—	20	60	mA	$T_J = +125^\circ\text{C}$, $V = V_{DRM} = V_{RRM}$
	Effective Thermal Resistance, Junction-to-Case	$R\theta_{JC}$	—	—	.023	$^\circ\text{C}/\text{Watt}$	Double-Side Cooled (DC)
	Critical Linear Rate-of-Rise of Forward Blocking Voltage (Higher values may cause device switching)	dv/dt	500	—	—	$\text{V}/\mu\text{sec}$	$T_J = +125^\circ\text{C}$, $V_{DRM} = .80$ Rated V_{RRM} Gate Open.
	Delay Time	t_d	—	1.5	—	μsec	Switching from 140 Volts, 20 Volt, 10 Ohm Gate 0.5 μsec Rise Time, $T_J = 25^\circ\text{C}$
	Gate Pulse Width Necessary To Trigger		—	—	10	μsec	$T_J = 25^\circ\text{C}$
	Gate Trigger Current	I_{GT}	—	120	—	mAdc	$T_C = 25^\circ\text{C}$, $V_D = 10$ Vdc, $R_L = 3$ Ohms
			5.0	30	—		$T_C = +125^\circ\text{C}$, $V_D = .5$ x Rated, $R_L = 1000$ Ohms
	Gate Trigger Voltage	V_{GT}	—	3.0	—	Vdc	$T_C = 0^\circ\text{C}$ to $+125^\circ\text{C}$, $V_D = 10$ Vdc, $R_L = 3$ Ohms
	Peak On-State Voltage	V_{TM}	—	—	1.45	Volts	$T_C = +125^\circ\text{C}$, $I_T = 1000$ Amps. Peak Duty Cycle $\leq 0.01\%$
	Conventional Circuit Commutated Turn-Off Time (With Reverse Voltage)	t_q	—	—	50	μsec	(1) $T_C = +125^\circ\text{C}$ (2) $I_T = 500$ Amps. (3) $V_R \geq 50$ Volts (4) 80% V_{DRM} Reapplied (5) Rate-of-Rise of Forward Blocking Voltage = 200 $\text{V}/\mu\text{sec}$ (6) Gate Bias = Open During Turn-Off Interval = 0 Volts, 100 Ohms (7) Duty Cycle $\leq 0.01\%$
	Conventional Circuit Commutated Turn-Off Time (With Feedback Diode)	t_q	—	55	60	μsec	(1) $T_C = +125^\circ\text{C}$ (2) $I_T = 500$ Amps. (3) $V_R = 2$ Volts Min. (4) 80% V_{DRM} Reapplied (5) Rate-of-Rise of Forward Blocking Voltage = 200 $\text{V}/\mu\text{sec}$. (6) Gate Bias = Open During Turn-Off Interval (7) Duty Cycle $\leq 0.01\%$



1. MAXIMUM ALLOWABLE PEAK ON-STATE CURRENT VS. PULSE WIDTH AT $T_C = 65^\circ\text{C}$



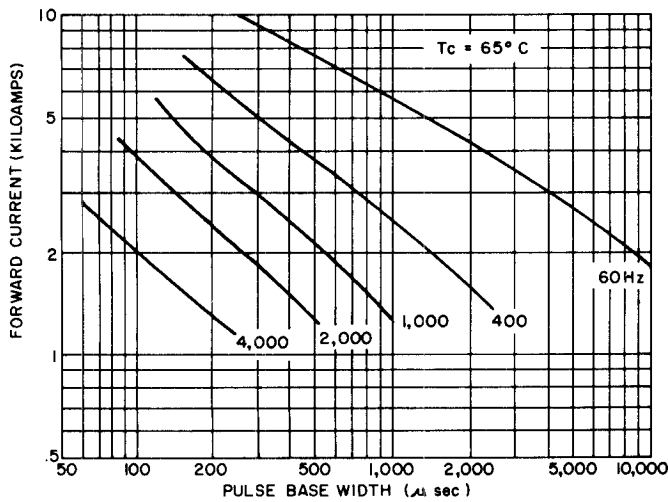
2. MAXIMUM ALLOWABLE PEAK ON-STATE CURRENT VS. PULSE WIDTH AT $T_C = 90^\circ\text{C}$



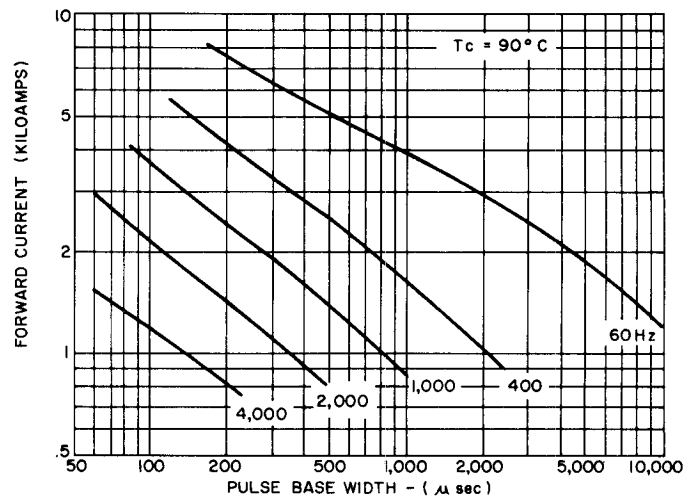
3. ENERGY PER PULSE FOR SINUSOIDAL PULSES

NOTES:

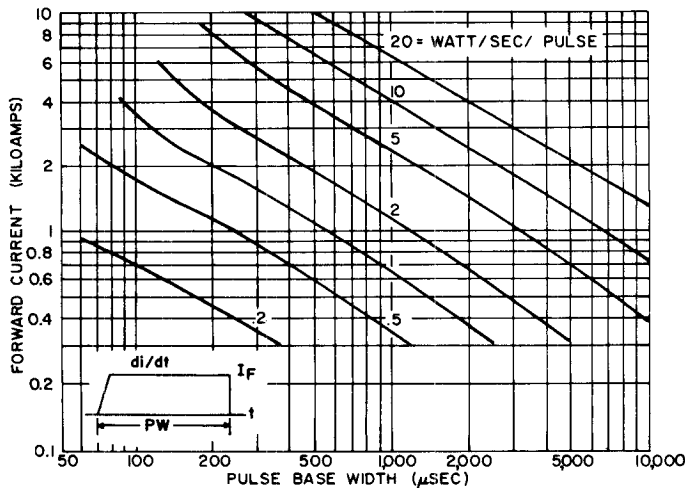
1. — Switching capability and losses with bypass diode.
2. Switching voltage from 15 Volts to 0.8 V_{DRM} .
3. Snubber discharge < 50 Amps. RC time constant $< 10 \mu\text{sec}$.
4. High gate drive, 20V/10 Ohms, 0.5 μsec rise time.



4. MAXIMUM ALLOWABLE PEAK ON-STATE CURRENT FOR TRAPEZOIDAL CURRENT WAVEFORMS FOR $T_C = 65^\circ\text{C}$



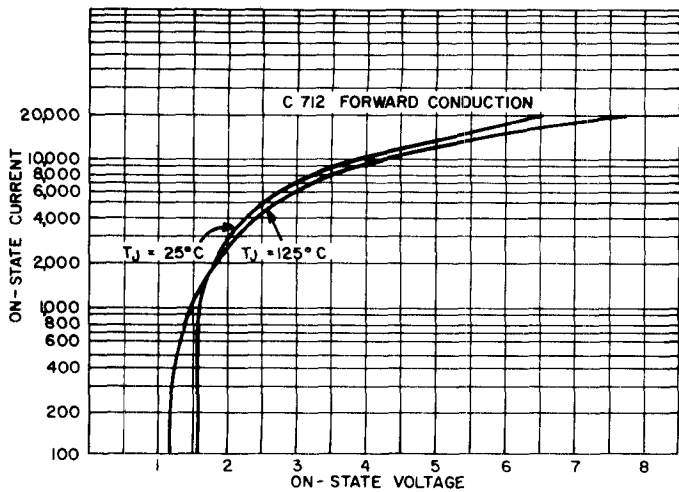
5. MAXIMUM ALLOWABLE PEAK ON-STATE CURRENT FOR TRAPEZOIDAL CURRENT WAVEFORMS FOR $T_C = 90^\circ\text{C}$



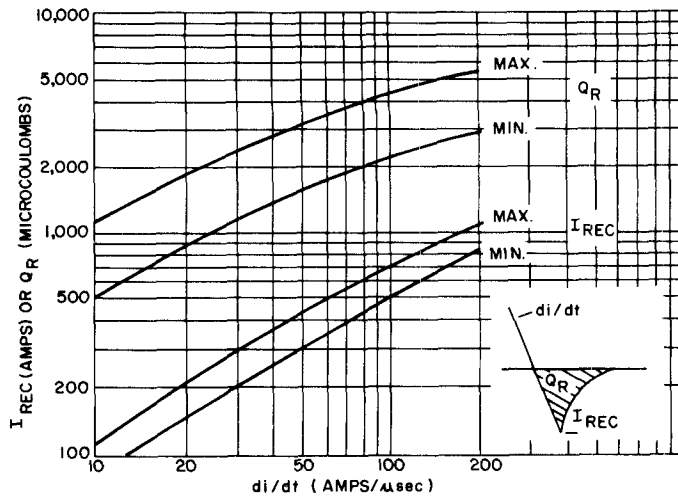
6. ENERGY PER PULSE FOR TRAPEZOIDAL CURRENT WAVEFORMS

NOTES:

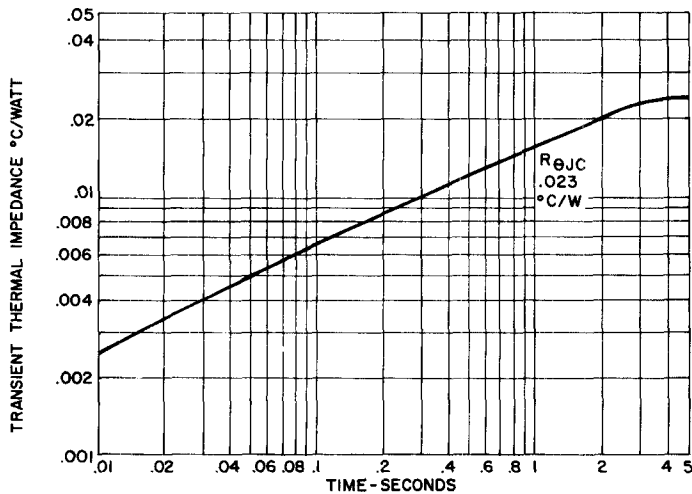
1. Switching voltage from 15 Volts to 0.8 V_{DRM} .
2. DI/DT during turn-on: 100A/ μsec .
3. Reverse voltage < 50 Volts. If no bypass diode is used, recovery switching losses must be added.
4. RC snubber time constant $< 10 \mu\text{sec}$.
5. High gate drive: 20V/10 Ohms, 0.5 μsec rise time.



7. FORWARD CONDUCTION CHARACTERISTIC ON-STATE



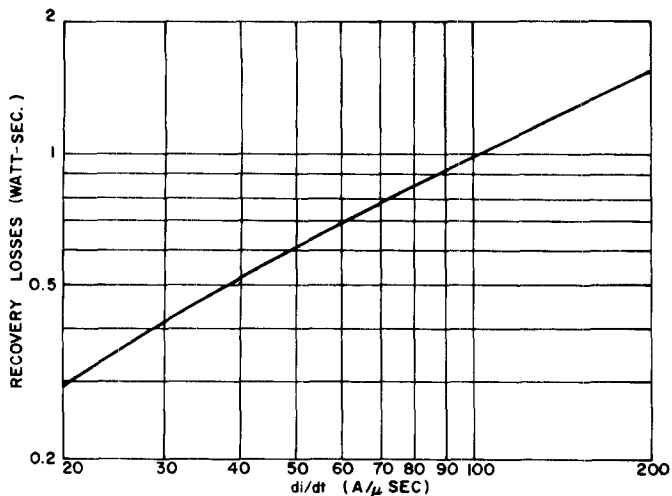
8. RECOVERED CHARGE (125°C)



9. TRANSIENT THERMAL RESISTANCE - JUNCTION-TO-CASE

NOTES:

1. Add .006°C/W to account for both case to dissipator interfaces when properly mounted; e.g., $R_{\theta JS} = .029^\circ \text{C/W}$. See Mounting Instructions.
2. DC Thermal Impedance is based on average full cycle junction temperature. Instantaneous junction temperature may be calculated using the following modifications:
 - end of conducting portion of cycle
 - 120° sq. wave add .0025°C/W along entire curve
 - 180° sq. wave add .0018°C/W along entire curve
 - 180° sine wave add .0010°C/W along entire curve
 - end of full cycle
 - any wave, subtract .001°C/W along entire curve



10. RECOVERY CURRENT SWITCHING LOSSES

NOTES:

If no bypass diode is used with this thyristor, the switching losses during recovery can be significant. The actual magnitude of these losses will vary widely depending on circuit conditions and snubber design. This curve represents typical recovery losses versus circuit di/dt. Since this curve is typical, it serves primarily to alert the equipment designer to the possible need for special design attention. The switching losses in a given circuit may be calculated with the following equation:

$$SLR = \int_0^{\infty} \bar{I}(t) \cdot V(t) dt$$

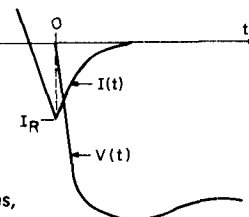
Where SLR is the recovery switching losses; $I(t)$ is the recovery current decay; $V(t)$ is the recovery voltage; and $t = 0$ occurs at the peak of the recovery current. $I(t)$ may be expressed as an exponential decay:

$$I(t) = I_R e^{-t/T}$$

Where I_R is the peak recovery current and $T = 2.5 \mu\text{sec}$. The junction temperature rise due to the recovery losses may be computed as follows:

$$\Delta T_j = F \cdot \sigma_{\pi} \cdot R_{\theta JA} + \alpha_{\pi} \cdot 3.5$$

Where σ_{π} is the recovery losses, $R_{\theta JA}$ is the DC junction to ambient thermal impedance, and F is the operating frequency.



OUTLINE DRAWING

